

MC68HC705C8

Addendum to MC68HC705C8 HCMOS Microcontroller Unit Technical Data

This addendum supplements *MC68HC705C8 Technical Data*, Rev. 1 (Motorola document number MC68HC705C8/D) with the following information:

- Corrections to *MC68HC705C8 Technical Data*
- Additional mechanical information for *MC68HC705C8 Technical Data*

CORRECTIONS MC68HC705C8/D, REV. 1

Corrections to the technical data manual are as follows:

1. Page 2-11, **Figure 2-4. OTPROM/EPROM Programming:**
 - a. There should only be one box labeled WAIT 1 ms.
 - b. YES label on output of NTRYS = 2 decision box should be NO.
2. Page 3-2, **3.1.3.1 COP RESET REGISTER:** Address of COP reset register should be \$001D.
3. Page 3-2, **3.1.3.2 COP CONTROL REGISTER:** The last sentence under the CME bit description should read as follows:

CME is readable and writable at any time.
4. Page 3-3, **3.1.3.2 COP CONTROL REGISTER:** The second sentence under the CM1 bit description should read as follows:

CM1 can be read anytime but may be written only once.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5. Page 3-3, **3.1.3.2 COP CONTROL REGISTER**: The second sentence under the CM0 bit description should read as follows:

CM0 can be read anytime, but may be written only once.

6. Page 3-10, (**3.3.1 STOP Mode**): The first three sentences from the paragraph at the top of the page should read as follows:

During the STOP mode, the I bit in the CCR is cleared to enable external interrupts.

7. Page 7-9, **Table 7-2. Opcode Map**: Bit Manipulation column heads BTB and BSC should be DIR and DIR.

8. Page 8-1, **8.2 THERMAL CHARACTERISTICS**: Thermal resistance of cerdip package should be 50 °C/W.

9. Page 8-3, **8.4 DC ELECTRICAL CHARACTERISTICS**:

- a. Pins specified under I/O Ports Hi-Z Leakage Current should be PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, RESET.
- b. Pins specified under Input Current should be $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.

10. Page 8-4, **8.5 DC ELECTRICAL CHARACTERISTICS**:

- a. Pins specified under I/O Ports Hi-Z Leakage Current should be PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, $\overline{\text{RESET}}$.
- b. Pins specified under Input Current should be $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.
- c. NOTE 3 should be
Run (Operating) I_{DD} and WAIT I_{DD} measured using external square wave clock source ($f_{OSC} = 2.0$ MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20$ pF on OSC2.

11. Page 8-7, **Figure 8-4. Total Current Drain vs Frequency** ($V_{DD} = 3.3$ V graph): Internal clock frequencies should read as follows:

0 250 kHz 500 kHz 750 kHz 1 MHz.

12. Page 8-11, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 720 ns.

13. Page 8-12, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 1500 ns.

**ADDITIONAL MECHANICAL DATA
MC68HC705C8 TECHNICAL DATA, REV. 1**

The following section supplements SECTION 9 of *MC68HC705C8 Technical Data*, REV. 1 with specifications of the 42-pin shrink dual in-line package (SDIP), the 44-pin quad flat pack (QFP), and the 44-lead ceramic-leaded chip carrier (CLCC). The information on pages 9-1 through 9-4 of *MC68HC705C8 Technical Data*, REV. 1 is still valid and **must not be removed**.

**SECTION 9
MECHANICAL DATA**

9.1 ORDERING INFORMATION

The following table provides additional ordering information for the MC68HC705C8 MCU.

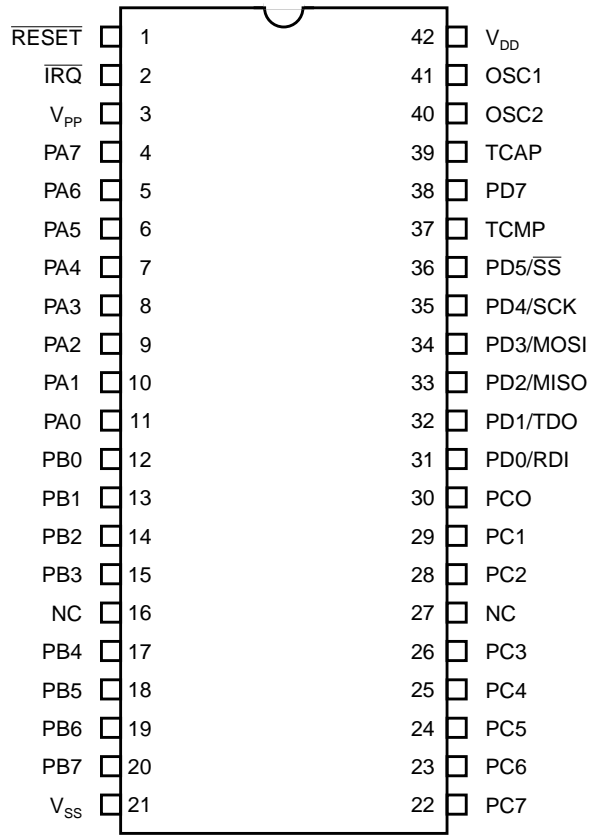
OTPROM MCUs

Package Type	Temperature Range	Order Number
Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C -40 °C to +85 °C	MC68HC705C8B MC68HC705C8CB
Quad Flat Pack (QFP)	0 °C to +70 °C -40 °C to +85 °C	MC68HC705C8FB MC68HC705C8CFB
Ceramic-Leaded Chip Carrier (CLCC)	0 °C to +70 °C -40 °C to +85 °C	MC68HC705C8FS MC68HC705C8CFS

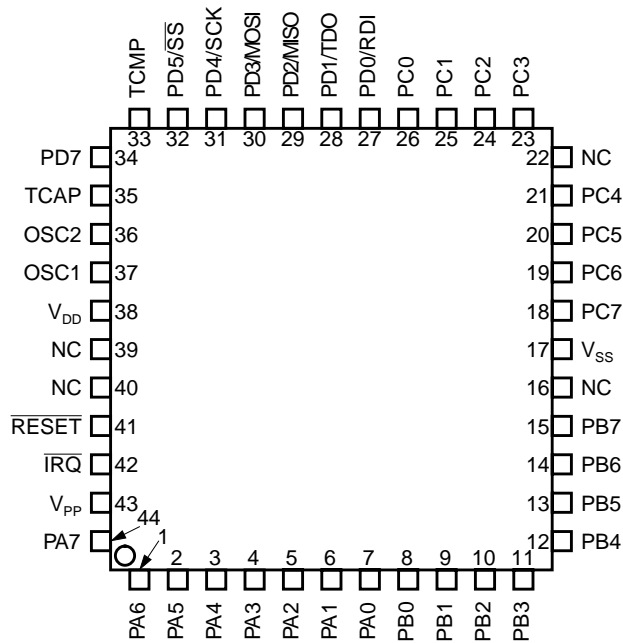
9.2 PIN ASSIGNMENTS

The following figures show the SDIP and QFP pin assignments.

9.2.3 42-Pin SDIP



9.2.4 44-Lead QFP



9.2.4 44-Lead CLCC

Pin assignments for this package are the same as for the 44-lead PLCC package.

9.3 PACKAGE DIMENSIONS

The MC68HC705C8 is available in a 42-pin shrink dual in-line package, a 44-lead quad flat pack (QFP) package, and a 44-lead ceramic-leaded chip carrier (CLCC) package. Package dimensions available at time of this publication are provided in this section. To make sure that you have the latest case outline specifications, contact one of the following:

- Local Motorola Sales Office
- Motorola Mfax
 - Phone 602-244-6609
 - EMAIL rmfax0@email.sps.mot.com
- Worldwide Web (wwweb) at <http://design-net.com>

Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.

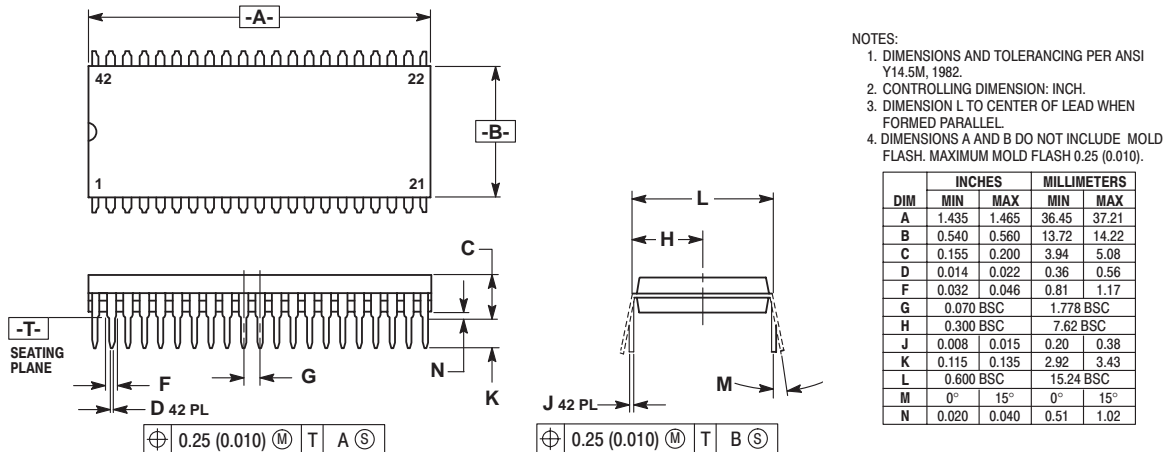


Figure 9-1. 42-Pin Shrink Dual In-Line Package (Case #858)

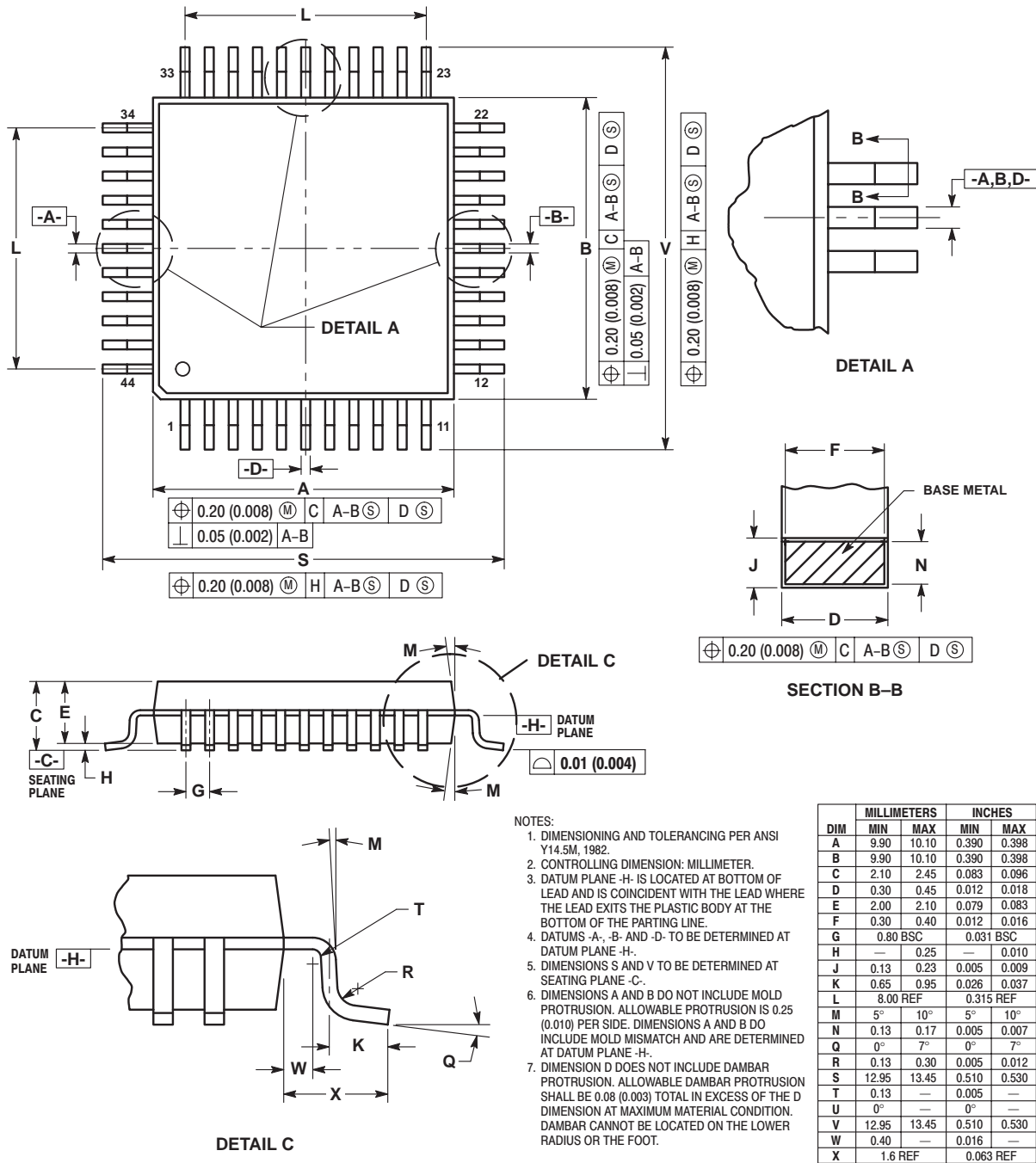


Figure 9-2. 44-Lead Quad Flat Pack (Case #824E)

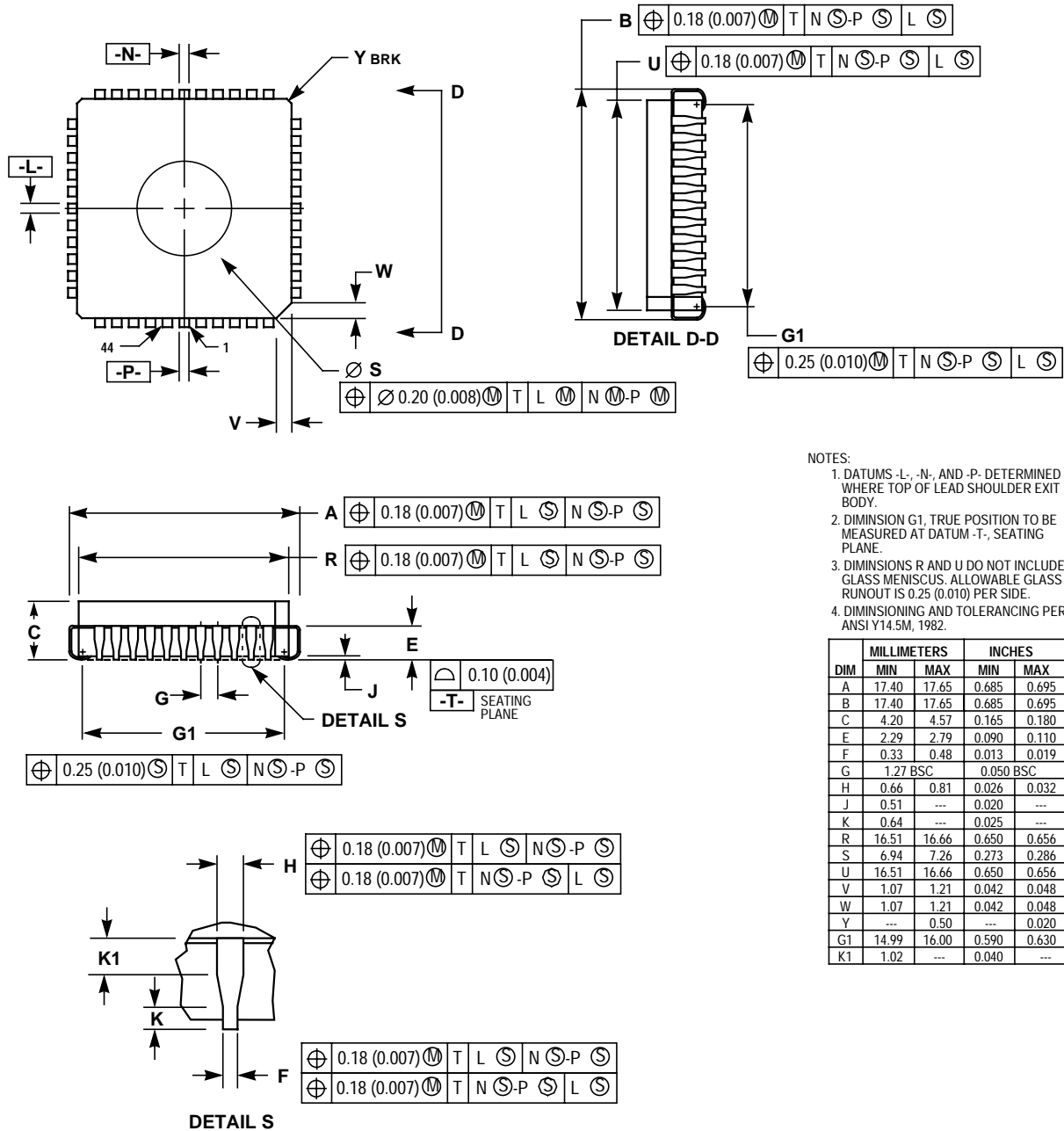


Figure 9-3. 44-Lead Ceramic-Leaded Chip Carrier (CLCC) (Case #777B)

Freescale Semiconductor, Inc.

Home Page:

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130

support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document. Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



For More Information On This Product,

Go to www.freescale.com

MC68HC705C8AD/D

